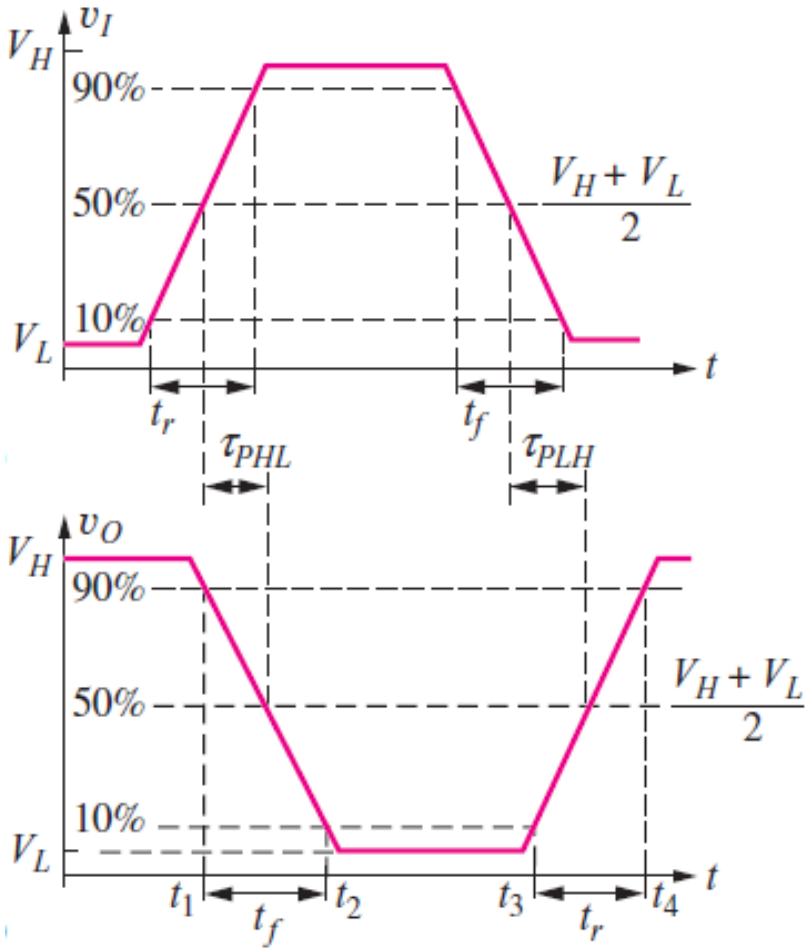
Announcements

- Homework 7 due Friday in class.
- Exam 2 being graded.
- Final project to be posted tonight.
  - XOR/LED as posted, but with some tweaks to specs, etc.

Logic Gate Dynamic Responses



- **Logic Swing:**

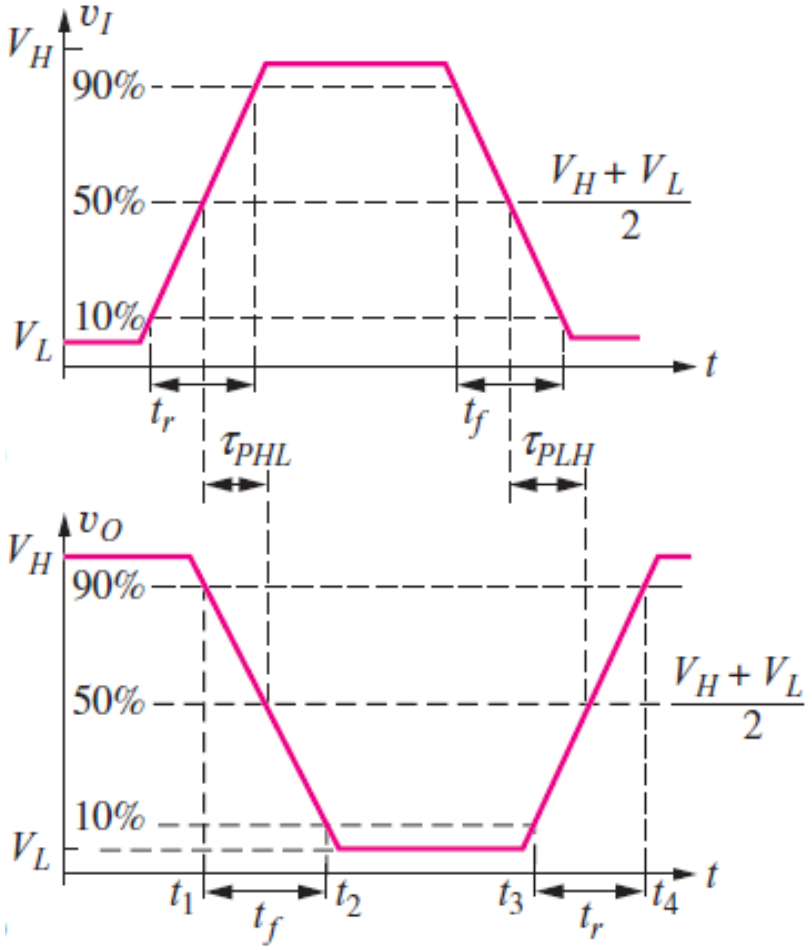
  $\Delta V = V_H - V_L$
- **10 percent point:**

  $V_{10\%} = V_L + 0.1\,\Delta V$
- **90 percent point:**

  $V_{90\%} = V_L + 0.9\,\Delta V$
- **50 percent point:**

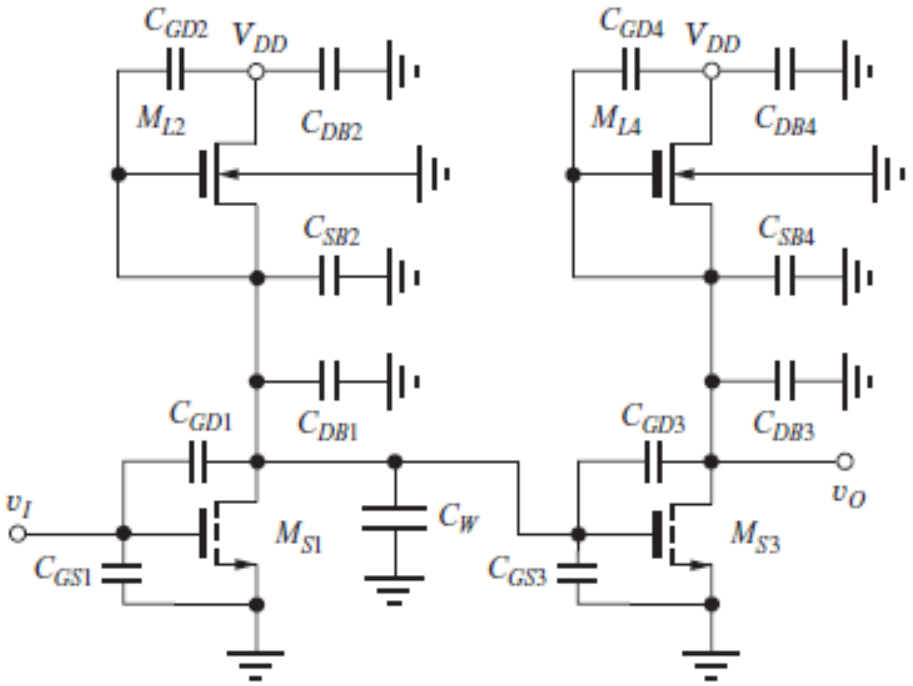
  $V_{50\%} = (V_L + V_H)/2$

Logic Gate Dynamic Responses

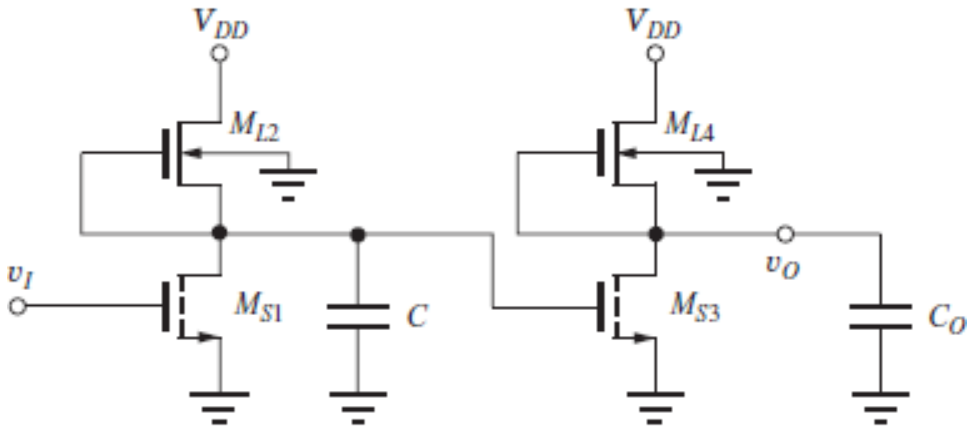


- **Rise time (t_r)**: time required from 10% point to 90% point
- **Fall time (t_f)**: time required from 90% point to 10% point
- **Propagation delay (τ_P)**: difference in time between the input and output signals reaching the 50% points
  - for output high-to-low: τ_{PHL}
  - for output low-to-high: τ_{PLH}
  - average propagation delay $\tau_P = (\tau_{PLH} + \tau_{PHL})/2$

Capacitances in Logic Circuits

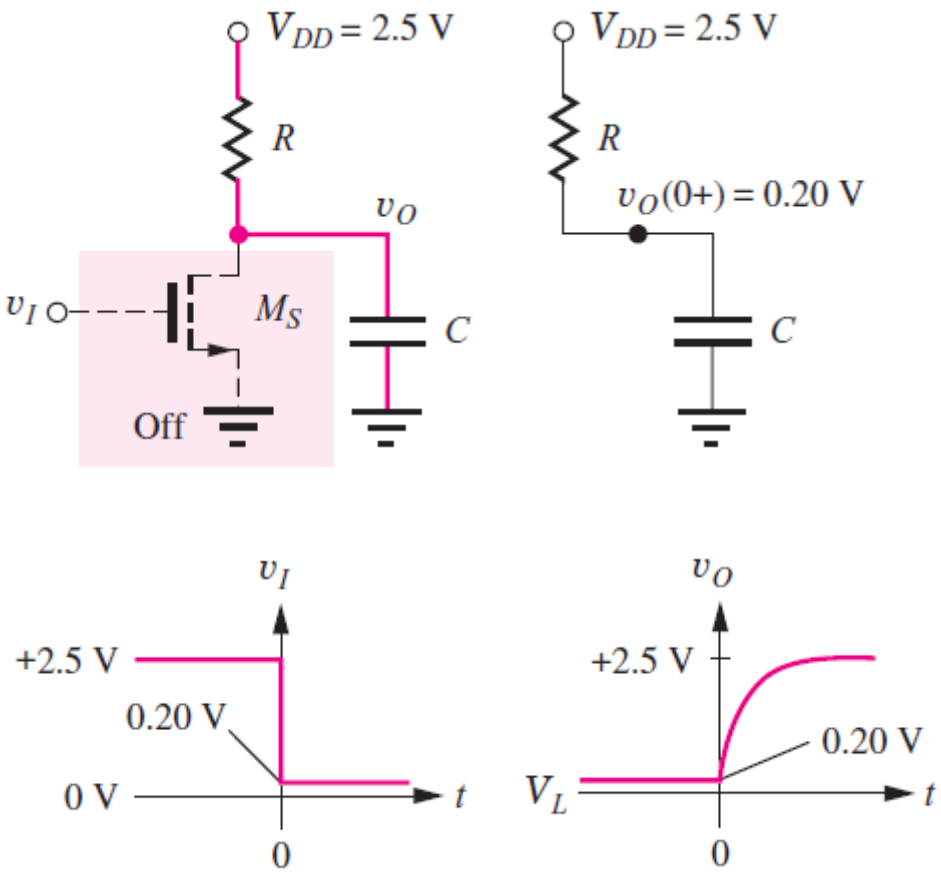


Various capacitances associated with transistors



The capacitances on a given node can be lumped into a fixed effective nodal capacitance *C*

Dynamic Response of NMOS Resistive Load Inverter

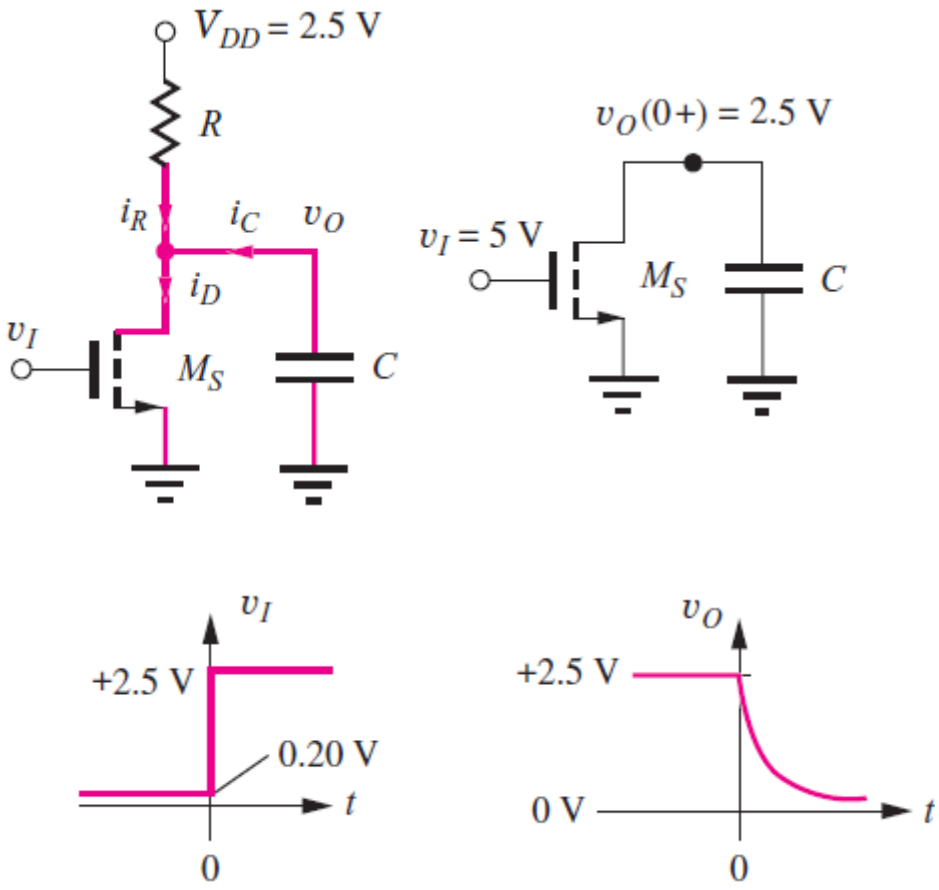


- Assume abrupt V_I change from V_H to V_L
- V_O changes from V_L to V_H by charging C via R
- From RC circuit basics

$$t_r = 2.2\ RC$$

$$\tau_{PLH} = 0.69\ RC$$

Dynamic Response of NMOS Resistive Load Inverter



- Assume abrupt V_I change from V_L to V_H
- V_O changes from V_H to V_L by discharging C via M_S
- R_{on} of M_S changes with time => use an effective resistance

$$R_{\text{eff}} = 1.7R_{\text{on}S}$$

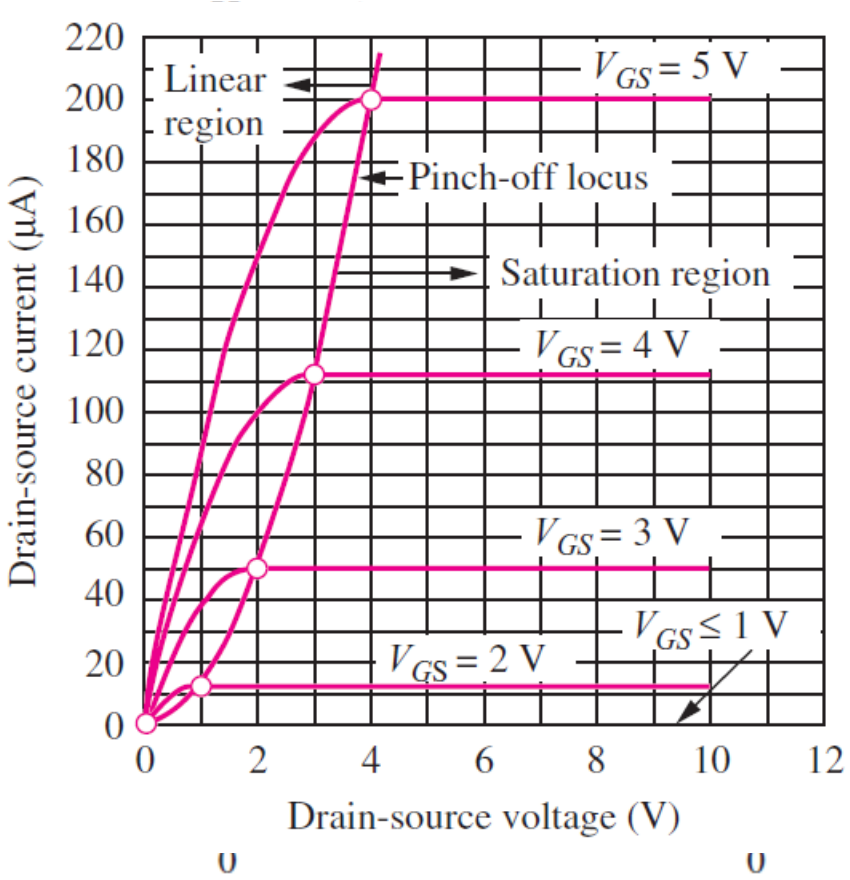
where $R_{\text{on}S} = [K_n(V_H - V_{TNS})]^{-1}$

- From RC circuit basics

$$t_f = 2.2\ R_{\text{eff}}C = 3.7R_{\text{on}S}C$$

$$\tau_{PHL} = 0.69R_{\text{eff}}C = 1.2R_{\text{on}S}C$$

Dynamic Response of NMOS Resistive Load Inverter



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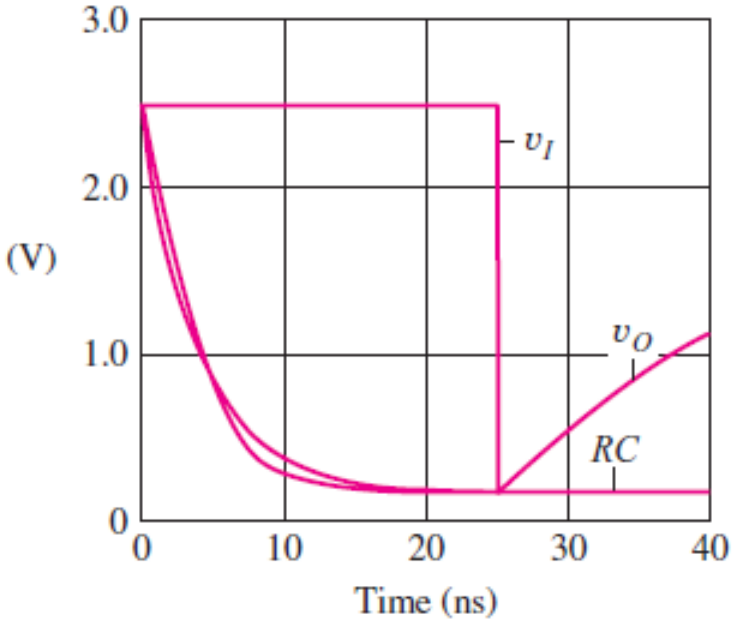
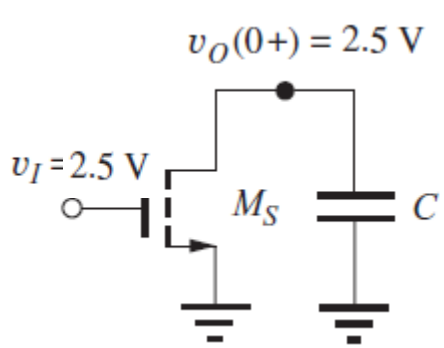
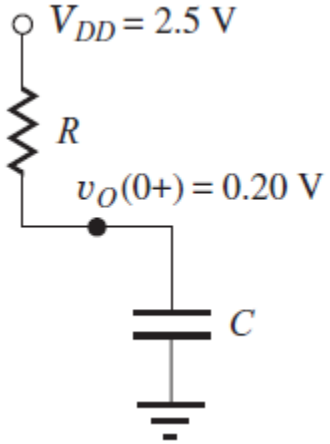
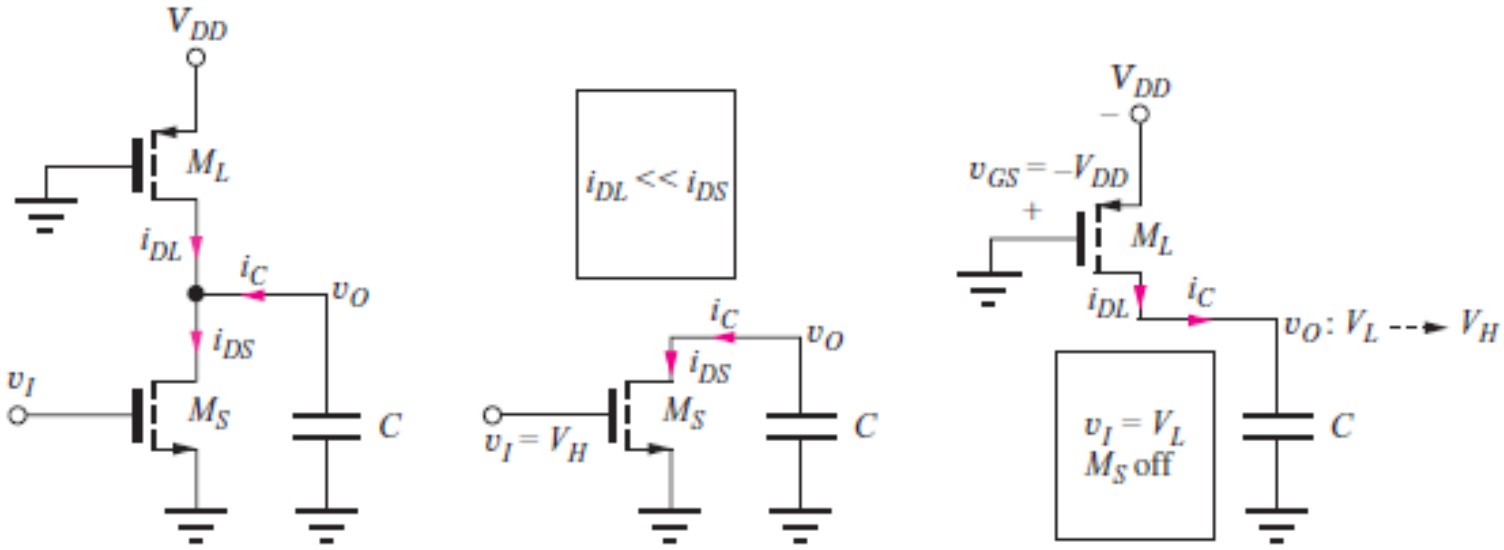






- Note the asymmetry in τ_{PLH} and τ_{PHL} ($\tau_{PHL} < \tau_{PLH}$)!
- Switching device must have a much smaller R_{on} than that of the load in order to produce the desired low logic level (V_L)

Dynamic Response of Inverters with Transistor Load Designs



- V_O changes from V_H to V_L by discharging C via M_S
- $t_f, \tau_{PHL} \propto R_{\mathrm{on}S}C$
- V_O changes from V_L to V_H by charging C via M_L
- $t_r, \tau_{PLH} \propto R_{\mathrm{on}L}C$, where $R_{\mathrm{on}L} = (K_L|V_{GS} - V_{TNL}|)^{-1}$

NMOS Inverter Delays

TABLE 6.10
NMOS Inverter Time Delays

	τ_{PHL}	τ_{PLH}	t_f	t_r
Resistor load	$1.2R_{onS}C$	$0.69RC$	$3.7R_{onS}C$	$2.2RC$
Pseudo NMOS	$1.2R_{onS}C$	$1.2R_{onL}C$	$3.7R_{onS}C$	$3.7R_{onL}C$
Depletion load	$1.2R_{onS}C$	$3.6R_{onL}C$	$3.7R_{onS}C$	$8.1R_{onL}C$
Saturated load	$1.2R_{onS}C$	$3.0R_{onL}C$	$3.7R_{onS}C$	$11.9R_{onL}C$
Linear load	$1.2R_{onS}C$	$0.69R_{onL}C$	$3.7R_{onS}C$	$3.7R_{onL}C$

$$R_{onS} = \frac{1}{K_S(V_H - V_{TNS})} \qquad R_{onL} = \frac{1}{K_L|V_{GS} - V_{TNL}|}$$

- t_f, τ_{PHL} are the same
- t_r, τ_{PLH} are different due to different current carrying capacity of load transistors

NMOS Performance Scaling

- $\tau_P = \frac{\tau_{PHL}+\tau_{PLH}}{2}$
  - $\tau_P \propto C$
  - $\tau_P \propto R_{\text{on}} \propto \left(\frac{W}{L}\right)^{-1}$

	τ_{PHL}	τ_{PLH}	t_f	t_r
Resistor load	$1.2R_{onS}C$	$0.69RC$	$3.7R_{onS}C$	$2.2RC$
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Linear load	$1.2R_{onS}C$	$0.69R_{onL}C$	$3.7R_{onS}C$	$3.7R_{onL}C$

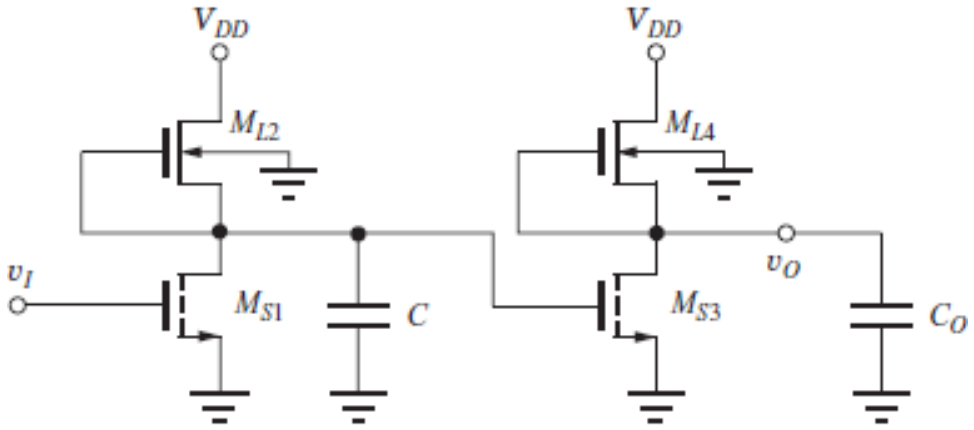
$$R_{onS} = \frac{1}{K_S(V_H - V_{TNS})} \qquad R_{onL} = \frac{1}{K_L|V_{GS} - V_{TNL}|}$$

- Delay is proportional to total load capacitance *C*, and inversely proportional to W/L.
- Larger size (larger W/L) => shorter delay, but larger power (last lecture: power scaling)

Switching Speed in Logic Circuits

- Can estimate switching time for capacitive load very simply:

$$i = C\frac{dv}{dt} \rightarrow \Delta t = \frac{C_{\text{total}}\Delta v}{i_{\text{avg}}} = \frac{\Delta Q}{i_{\text{avg}}}$$



- Δv is voltage swing
- Estimate i_{avg} using trapezoidal rule: i_{avg}=(i_{init}+ i_{final})/2
  - Can improve estimate by using $\Delta t = \Delta t_1 + \Delta t_2 + \cdots$ associated with $\Delta v = \Delta v_1 + \Delta v_2 + \cdots$